PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2000-223417**

(43)Date of publication of application : **11.08.2000**

(51)Int.Cl. H01L 21/205

(21)Application number : **11-019651**

(22)Date of filing : **28.01.1999**

(71)Applicant : **SONY CORP**

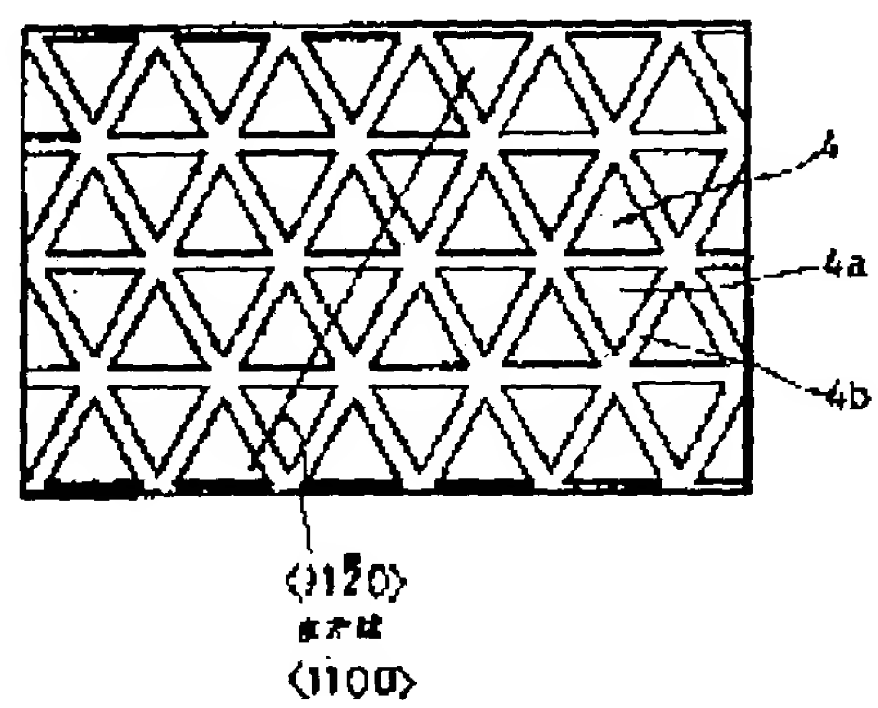
(72)Inventor : **TOMIOKA SATOSHI**

(54) **GROWING METHOD OF SEMICONDUCTOR, MANUFACTURE OF SEMICONDUCTOR SUBSTRATE, AND MANUFACTURE OF SEMICONDUCTOR DEVICE**

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method of growing a semiconductor, such as a nitride III-V compound semiconductor on a substrate that has a lattice constant and a thermal expansion coefficient, different from those of the semiconductor without producing warpage or fissures, and a method of manufacturing a semiconductor substrate and a semiconductor device by the use of this growing method of a semiconductor.

SOLUTION: In a semiconductor growing method, where a nitride III-V compound semiconductor such as a GaN semiconductor is formed on a substrate, such as a sapphire substrate formed of a material different from that of the compound semiconductor using a growing mask, a growing mask 4 which contains at least a pattern that is threefold or sixfold symmetrical is used as the growing mask. A pattern which is threefold symmetrical is a regular triangle, and a pattern which is sixfold symmetrical is a regular hexagon. In this way, a nitride III-V compound semiconductor thick layer is selectively grown, and then the substrate is removed by lapping or the like so as to obtain only the nitride III-V compound semiconductor layer, and a semiconductor device such as a GaN semiconductor laser is manufactured using the compound semiconductor layer as a substrate.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The growth technique of the semiconductor characterized by using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as the above-mentioned growth mask in part in the growth technique of a semiconductor of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.
[Claim 2] The growth technique of the semiconductor according to claim 1 characterized by using the growth mask which consists of a repeat pattern of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as the above-mentioned growth mask.
[Claim 3] The above-mentioned semiconductor is the growth technique of the semiconductor according to claim 1 characterized by being a nitride system III-V group compound semiconductor.
[Claim 4] The growth technique of the semiconductor according to claim 3 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the halide vapor-phase-epitaxial-growth method or the hydride vapor-phase-epitaxial-growth method.
[Claim 5] The growth technique of the semiconductor according to claim 3 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the organic metalization study vapor growth.
[Claim 6] The growth technique of the semiconductor according to claim 3 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the molecular-beam-epitaxy method.
[Claim 7] The above-mentioned substrate is the growth technique of the semiconductor according to claim 3 characterized by being the substrate which consists of sapphire, silicon carbide, a zinc oxide, a spinel, silicon, or a **-ized gallium.
[Claim 8] The above-mentioned growth mask is the growth technique of the semiconductor according to claim 3 characterized by consisting of a dielectric.
[Claim 9] The above-mentioned growth mask is the growth technique of the semiconductor according to claim 3 characterized by consisting of a silicon dioxide, silicon nitride, or an aluminum oxide.
[Claim 10] The above-mentioned growth mask is the growth technique of the semiconductor according to claim 3 characterized by consisting of a cascade screen of at least two layers chosen out of the group which consists of a silicon-dioxide layer, a silicon-nitride layer, and an aluminum-oxide layer.
[Claim 11] The above-mentioned growth mask is the growth technique of the semiconductor according to claim 3 characterized by consisting of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel.
[Claim 12] The above-mentioned growth mask is the growth technique of the semiconductor according to claim 3 characterized by consisting of a cascade screen of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel, and a dielectric film.
[Claim 13] The above-mentioned growth mask is the growth technique of the semiconductor according to claim 3 characterized by being formed so that the plane of composition of the above-mentioned nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side.
[Claim 14] The manufacture technique of the semiconductor substrate characterized by using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as the above-mentioned growth mask in part in the manufacture technique of a semiconductor substrate of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.
[Claim 15] The manufacture technique of the semiconductor substrate according to claim 14 characterized by using the growth mask which consists of a repeat pattern of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as the above-mentioned growth mask.
[Claim 16] The above-mentioned semiconductor is the manufacture technique of the semiconductor substrate according to claim 14 characterized by being a nitride system III-V group compound semiconductor.
[Claim 17] The manufacture technique of the semiconductor substrate according to claim 16 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the halide vapor-phase-epitaxial-growth method or the hydride vapor-phase-epitaxial-growth method.
[Claim 18] The manufacture technique of the semiconductor substrate according to claim 16 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the organic metalization study vapor growth.
[Claim 19] The manufacture technique of the semiconductor substrate according to claim 16 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the molecular-beam-epitaxy method.
[Claim 20] The above-mentioned substrate is the manufacture technique of the semiconductor substrate according to claim 16

characterized by being the substrate which consists of sapphire, silicon carbide, a zinc oxide, a spinel, silicon, or a **-ized gallium.
[Claim 21] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 16 characterized by consisting of a dielectric.
[Claim 22] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 16 characterized by consisting of a silicon dioxide, silicon nitride, or an aluminum oxide.
[Claim 23] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 16 characterized by consisting of a cascade screen of at least two layers chosen out of the group which consists of a silicon-dioxide layer, a silicon-nitride layer, and an aluminum-oxide layer.
[Claim 24] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 16 characterized by consisting of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel.
[Claim 25] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 16 characterized by consisting of a cascade screen of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel, and a dielectric film.
[Claim 26] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 16 characterized by being formed so that the plane of composition of the above-mentioned nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side.
[Claim 27] The manufacture technique of the semiconductor substrate according to claim 14 characterized by removing the above-mentioned substrate after carrying out the selective growth of the above-mentioned semiconductor.
[Claim 28] The manufacture technique of the semiconductor substrate according to claim 14 characterized by removing the above-mentioned substrate by a wrapping or etching after carrying out the selective growth of the above-mentioned semiconductor.
[Claim 29] The manufacture technique of the semiconductor device characterized by using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as the above-mentioned growth mask in part in the manufacture technique of a semiconductor device of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.
[Claim 30] The manufacture technique of the semiconductor device according to claim 29 characterized by using the growth mask which consists of a repeat pattern of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as the above-mentioned growth mask.
[Claim 31] The above-mentioned semiconductor is the manufacture technique of the semiconductor device according to claim 29 characterized by being a nitride system III-V group compound semiconductor.
[Claim 32] The manufacture technique of the semiconductor device according to claim 31 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the halide vapor-phase-epitaxial-growth method or the hydride vapor-phase-epitaxial-growth method.
[Claim 33] The manufacture technique of the semiconductor device according to claim 31 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the organic metalization study vapor growth.
[Claim 34] The manufacture technique of the semiconductor device according to claim 31 characterized by growing up the above-mentioned nitride system III-V group compound semiconductor by the molecular-beam-epitaxy method.
[Claim 35] The above-mentioned substrate is the manufacture technique of the semiconductor device according to claim 31 characterized by being the substrate which consists of sapphire, silicon carbide, a zinc oxide, a spinel, silicon, or a **-ized gallium.
[Claim 36] The above-mentioned growth mask is the manufacture technique of the semiconductor device according to claim 31 characterized by consisting of a dielectric.
[Claim 37] The above-mentioned growth mask is the manufacture technique of the semiconductor device according to claim 31 characterized by consisting of a silicon dioxide, silicon nitride, or an aluminum oxide.
[Claim 38] The above-mentioned growth mask is the manufacture technique of the semiconductor substrate according to claim 31 characterized by consisting of a cascade screen of at least two layers chosen out of the group which consists of a silicon-dioxide layer, a silicon-nitride layer, and an aluminum-oxide layer.
[Claim 39] The above-mentioned growth mask is the manufacture technique of the semiconductor device according to claim 31 characterized by consisting of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel.
[Claim 40] The above-mentioned growth mask is the manufacture technique of the semiconductor device according to claim 31 characterized by consisting of a cascade screen of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel, and a dielectric film.
[Claim 41] The above-mentioned growth mask is the manufacture technique of the semiconductor device according to claim 31 characterized by being formed so that the plane of composition of the above-mentioned nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side.
[Claim 42] The manufacture technique of the semiconductor device according to claim 29 characterized by removing the above-mentioned substrate after carrying out the selective growth of the above-mentioned semiconductor.
[Claim 43] The manufacture technique of the semiconductor device according to claim 29 characterized by removing the above-mentioned substrate by a wrapping or etching after carrying out the selective growth of the above-mentioned semiconductor.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention is applied to a manufacture of the semiconductor laser, the light emitting diode, or the electronic run element using the nitride system III-V group compound semiconductor about the growth technique of a semiconductor, the manufacture technique of a semiconductor substrate, and the manufacture technique of a semiconductor device, and is suitable.
[0002]
[Description of the Prior Art] In recent years, the development of semiconductor light emitting devices, such as semiconductor laser which can obtain the photogenesis to an ultraviolet region from a visible region, and light emitting diode, is actively performed using nitride system III-V group compound semiconductors, such as AlGaInN. It is asked for utilization of the semiconductor laser from which photogenesis of a short wavelength region is obtained in order to raise recording density, such as an optical disk, in the field of optical recording also especially in it.
[0003] Recently, in AlGaInN system semiconductor laser, the continuous oscillation of 300 hours in a room temperature is attained by growing up a nitride system III-V group compound semiconductor layer by the organic metalization study vapor-growth (MOCVD) method through the buffer layer which consists of a gallium nitride (GaN) on silicon on sapphire (Jpn.J.Appl.Phys.35, L74 (1996), Jpn.J.Appl.Phys.36, L1059 (1997)). However, the nitride system III-V group compound semiconductor layer grown up on silicon on sapphire since silicon on sapphire differed also in a lattice constant and a coefficient of thermal expansion greatly from GaN is 1x108 to 1x109. An individual / cm2 It has the penetration trusion (trusion which the trusion defect spread and ran through under the crystal) of a grade, and when this produces a light emitting device, it is the factor which determines the life. Therefore, in order to realize the practical life of 10,000 hours or more, it is required to reduce the density of this penetration trusion, and various studies are made until now.
[0004] For example, although one of them has use of GaN substrate The technique of the present leading ** being carried out as the manufacture technique of GaN substrate Grow up GaN layer through a buffer layer on silicon on sapphire, and the growth mask which formed the silicon-dioxide (SiO2) layer of the shape of a stripe of 1-4 micrometer width of face in the 7-micrometer pitch is formed on it. After making longitudinal direction carry out the selective growth of the GaN layer by the chloride vapor-phase-epitaxial-growth method on silicon on sapphire using this growth mask, GaN substrate is manufactured by removing silicon on sapphire (Jpn.J.Appl.Phys.36 and L899 (1997)). It is the density of the penetration trusion of GaN layer which grew on the growth mask according to this technique, i.e., GaN substrate, 1x107 An individual / cm2 It can decrease even to a grade.
[0005]
[Problem(s) to be Solved by the Invention] However, by the manufacture technique of the above-mentioned conventional GaN substrate, asymmetry by the coefficient-of-thermal-expansion difference with silicon on sapphire becomes large as a growth thickness increases, although it decreases, and curvature and a crack produce the density of the penetration trusion of a growth phase at the time of the temperature fall after a crystal growth. For this reason, a chip and a crack will increase at the time of a wrapping at the elimination process of silicon on sapphire, and the manufacture yield of a substrate will become very low. Moreover, when a light emitting device was produced on this GaN substrate that curved, there were various problems -- the depth of focus of an aligner cannot correspond to curvature -- at the time of the exposure in the photo-lithography process performed after a crystal growth.
[0006] Therefore, even if the purpose of this invention grows up the thick film of semiconductors, such as a nitride system III-V group compound semiconductor, on the substrate from which a lattice constant and a coefficient of thermal expansion are different, it is to offer the growth technique of the semiconductor which neither curvature nor a crack generates, the manufacture technique of the semiconductor substrate using this growth technique, and the manufacture technique of a semiconductor device.
[0007]
[Means for Solving the Problem] If according to the study of this invention person the crack and curvature of the growth phase which is the trouble of the above-mentioned conventional technique have the critical point in the stress generated in the growth phase according to the coefficient-of-thermal-expansion difference with a substrate and stress exceeds it, a crack will arise in a growth phase, and when stress is less than [it], it is discovered as curvature. And as a result of inquiring zealously, it found out that it was regular in the orientation which this crack produces. Specifically by the growth phase which consists of nitride system III-V group compound semiconductors, such as GaN, it found out generating a crack in parallel with the {11-20} **** or {1-100} ****. Moreover, when this invention person grew up the semiconductor alternatively through the growth mask which has a stripe-like pattern, he found out that the crack of the orientation in alignment with the stripe decreased.
[0008] The crack and curvature of a growth phase decrease sharply by forming a growth mask so that the plane of composition of the nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side from these things. What specifically consists of a pattern which has the symmetry or symmetric property symmetrical with 6 times 3

times as such a growth mask is effective.
[0009] Furthermore, the above thing may be similarly materialized, when growing up semiconductors other than a nitride system III-V group compound semiconductor, as long as the same property is shown.
[0010] This invention is thought out based on the above studies by this invention person.
[0011] That is, in order to attain the above-mentioned purpose, it is characterized by for invention of the 1st of this invention using a growth mask, and using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part in the growth technique of a semiconductor of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor.
[0012] It is characterized by invention of the 2nd of this invention using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part in the manufacture technique of a semiconductor substrate of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.
[0013] It is characterized by invention of the 3rd of this invention using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part in the manufacture technique of a semiconductor device of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.
[0014] In this invention, what consists of a repeat pattern of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask typically is used. Although this growth mask consists only of what consists only of a pattern which has symmetric property symmetrical with 3 times, and a pattern which has symmetric property symmetrical with 6 times, the pattern which has symmetric property symmetrical with others and 3 times, and the pattern which has symmetric property symmetrical with 6 times may be intermingled.
[0015] Typically in this invention, the semiconductor which should carry out a selective growth is a nitride system III-V group compound semiconductor. Specifically, this nitride system III-V group compound semiconductor consists of at least one kind of III group element chosen out of the group which consists of a gallium (Ga), aluminum (aluminum), an indium (In), boron (B), and a thallium (Tl), and a V group element which contains an arsenic (As) or Lynn (P) further by the case, including nitrogen (N) at least. When the example of this nitride system III-V group compound semiconductor is given, they are GaN, AlGaN, AlN, GaInN, AlGaInN, InN, etc.
[0016] In this invention, the halide vapor-phase-epitaxial-growth method (a chloride vapor-phase-epitaxial-growth method is the kind) a growth rate is quick, or a hydride vapor-phase-epitaxial-growth method (all are called "HVPE method".) is suitably used for the selective growth of a nitride system III-V group compound semiconductor. Here, a halide vapor-phase-epitaxial-growth method means the vapor growth which a halogen contributes to transportation or a reaction. You may use an organic metalization study vapor-growth (MOCVD) method, a molecular-beam-epitaxy (MBE) method, etc. for the selective growth of a nitride system III-V group compound semiconductor.
[0017] In this invention, although what was chosen as a substrate according to the semiconductor which should carry out a selective growth is used, when carrying out the selective growth of the nitride system III-V group compound semiconductor especially, what consists of sapphire, silicon carbide (SiC), a zinc oxide (ZnO), a spinel, silicon (Si), a **-ized gallium (GaAs), etc. is used suitably. As a growth mask, specifically Moreover, a dielectric (SiO2), for example, a silicon dioxide, What consists of silicon nitride (SiN), an aluminum oxide (aluminum2 O3), etc., The cascade screen of at least two layers chosen out of the group which consists of a layer of these dielectrics, IVa group's metals (Ti, Zr, Hf, etc.), and Va group's metal (it Nbs V --) What [consists of the metal membrane or alloy layer which consists of at least one kind of metals chosen out of the group which consists of VIa group's metals (Cr, Mo, W, etc.) and nickel, such as Ta,] What consists of a cascade screen of the metal membrane or alloy layer which consists of at least one kind of metal chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel, and a dielectric film is used.
[0018] In this invention, when the semiconductor which should carry out a selective growth is a nitride system III-V group compound semiconductor, a growth mask is formed so that the plane of composition of the nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side.
[0019] In the 2nd of this invention, and the 3rd invention, typically, after carrying out the selective growth of the semiconductor, a wrapping, etching, etc. remove a substrate.
[0020] In this invention constituted as mentioned above By using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part When the selective growth of the nitride system III-V group compound semiconductor is carried out on a substrate using this growth mask, In the fraction of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times among growth masks at least Since the plane of composition of the nitride system III-V group compound semiconductor which carries out a selective growth turns into {11-20} side or {1-100} side from each opening of a growth mask, the stress by the coefficient-of-thermal-expansion difference with a substrate is eased, and a growth phase can reduce curvature and crack initiation. For this reason, even if it grows up a thick film, occurrence of the crack or curvature can be prevented.
[0021]
[Embodiments of the Invention] Hereafter, it explains, referring to a drawing about the operation gestalt of this invention. In addition, in the complete diagram of the operation gestalt, the same sign is given to an identity or a corresponding fraction.
[0022] First, the manufacture technique of GaN system semiconductor laser by the 1st operation gestalt of this invention is explained. This manufacture technique is shown in drawing 1 - view 8 . This GaN system semiconductor laser has SCH (Separate Confinement Heterostructure) structure.
[0023] In this 1st operation gestalt, first, as shown in drawing 1 , Cth page silicon on sapphire 1 is prepared, and thickness grows up GaN buffer layer 2 which is 30nm at the temperature of 520 degrees C for example, by the MOCVD method on it. This GaN buffer layer

2 consists of a near crystal layer amorphously, and serves as the nucleus at the time of growing up a substratum layer on it. In growth of this GaN buffer layer 2, trimethylgallium (CH3) (3 Ga) gas and ammonia (NH3) gas are used as material gas, for example. Next, thickness grows up the substratum GaN layer 3 which is 2 micrometers at the temperature of 1020 degrees C for example, by the MOCVD method on this GaN buffer layer 2.

[0024] Next, SiO2 whose thickness is 0.1 micrometers at the temperature of 450 degrees C by CVD on the substratum GaN layer 3 as shown in drawing 2 This SiO2 after forming a layer Patterning of the layer is carried out by the photo-lithography method and the etching method, and the growth mask 4 of a pattern configuration which is shown in drawing 3 is formed. As shown in drawing 3 , this growth mask 4 has the mask pattern by which opening 4a of an equilateral-triangle pattern which has symmetric property symmetrical with 3 times was arranged through mask section 4b of predetermined width of face. The side of the pattern of the equilateral triangle which constitutes this growth mask 4 is made to become parallel to the <11-20> orientation of Cth page silicon on sapphire 1, or the <1-100> orientation here. Moreover, the length of the side of opening 4a of the equilateral triangle of this growth mask 4 is set to 7 micrometers, and width of face of mask section 4b between them is set to 3 micrometers.

[0025] Next, an acetone (CH3 COCH3) and a methanol (CH3 OH) wash the Cth page silicon on sapphire 1 in which the growth mask 4 was formed, and further, after dipping in the diluted hydrochloric acid (HCl) or the diluted fluoric acid (HF) about 10 seconds, a pure water washes, for example.

[0026] Next, as shown in drawing 4 , the selective growth of the GaN layer 5 is carried out to longitudinal direction at the temperature of 1000 degrees C by the chloride vapor-phase-epitaxial-growth method, using the growth mask 4. In the selective growth of this GaN layer 5, after, heating Cth page silicon on sapphire 1 to 1000 degrees C for example, passing ammonia (NH3) gas by 11. the flow rate for /, on a metal Ga, hydrogen chloride (HCl) gas is passed and gallium-chloride (GaCl) gas is supplied. As for the conditions of supply of GaCl gas, a growth rate is made to become o'clock in about 40micrometers /. In the case of this selective growth, the plane of composition of GaN layer which carries out a selective growth to longitudinal direction on mask section 4b from on the substratum GaN layer 3 of each opening 4a of the growth mask 4 When the side of opening 4a of the equilateral triangle of the growth mask 4 is parallel to the <11-20> orientation of Cth page silicon on sapphire 1, it becomes {11-20} side of GaN. When the side of opening 4a of the equilateral triangle of the growth mask 4 is parallel to the <1-100> orientation of Cth page silicon on sapphire 1, it becomes {1-100} side of GaN. If the selective growth of the 1 hour GaN is carried out on these conditions, the GaN layer 5 of the thick film of the single crystal with thickness quality [the low crystal-defect density with a flat front face] at about 40 micrometers will be obtained. The orientation relationship of Cth page silicon on sapphire 1 and the GaN layer 5 is shown in drawing 5 .

[0027] Thus, the place, the curvature, or crack initiation which observed the GaN layer 5 by which the selective growth was carried out with the light microscope were not seen.

[0028] Next, as shown in drawing 6 , by wrapping mechanically, it removes and only the GaN layer 5 by which the selective growth was carried out is taken out for Cth page silicon on sapphire 1 etc. from the rear-face side.

[0029] Next, as shown in drawing 7 , the GaN layer 5 of the thick film which does in this way and was obtained is used as a GaN substrate. On it by for example, the MOCVD method The n type AlGaN clad layer 6, the n type GaN lightguide 7 8, for example, the barrier layer of Ga1-x Inx N/Ga1-y Iny N multiplex quantum well structure, the p type AlGaN cap layer 9, the p type GaN lightguide 10, the p type AlGaN clad layer 11 And the p type GaN contact layer 12 is grown up one by one. Here, since the GaN layer 5 used as the substratum of these layers is a single crystal with a quality low crystal-defect density, these layers also serve as the single crystal with a quality low crystal-defect density. Growth temperature of the n type AlGaN clad layer 6 which is a layer which does not contain In here, the n type GaN lightguide 7, the p type AlGaN cap layer 9, the p type GaN lightguide 10, the p type AlGaN clad layer 11, and the p type GaN contact layer 12 is made into about 1000 degrees C. Growth temperature of the barrier layer 8 of the Ga1-x Inx N/Ga1-y InyN multiplex quantum well structure which is a layer containing In is made into 700-800 degrees C. Moreover, as for example, a Ga raw material, ammonia (NH3) is used for the growth raw material of these GaN system semiconductor layers as trimethylindium (CH3) (3In) and an N raw material as a trimethylaluminum (CH3) (3 aluminum) and an In raw material as trimethylgallium (CH3) (3 Ga) and an aluminum raw material. Moreover, as carrier gas, the mixed gas of hydrogen (H2) and nitrogen (N2) is used, for example. As an n type dopant, for example, methylcyclopentadienyl magnesium (MCp) (2 Mg) is used for a dopant as a mono silane (SiH4) and a p type dopant. moreover -- if an example of these layer thicknesss is given -- the n type AlGaN clad layer 6 -- in 0.5 micrometers and the n type GaN lightguide 7, 0.1 micrometers and the p type AlGaN cap layer 9 set [20nm and the p type GaN lightguide 10] 0.5 micrometers and the p type GaN contact layer 12 to 0.5 micrometers for 0.1 micrometers and the p type AlGaN clad layer 11 Then, heat treatment for an electric activation of the acceptor doped by the p type AlGaN cap layer 9, the p type GaN lightguide 10, the p type AlGaN clad layer 11, and the p type GaN contact layer 12 is performed. Temperature of this heat treatment is made into about 700 degrees C.

[0030] Next, as shown in drawing 8 , after forming the resist pattern (not shown) of the stripe configuration of predetermined width of face on the p type GaN contact layer 12, it etches by the reactive-ion-etching (RIE) method by Mr. Fukashi in the middle of the thickness orientation of the p type AlGaN clad layer 11, using this resist pattern as a mask, and the ridge section is formed.

[0031] Next, while the p lateral electrode 13 which consists of a nickel/Pt/Au layer is formed on the p type GaN contact layer 12 of the ridge section, the n lateral electrode 14 which consists of a Ti/aluminum/Pt/Au layer is formed in the rear face of the GaN layer 5, i.e., GaN substrate.

[0032] Then, after processing the GaN layer 5 in which laser structure was formed as mentioned above, i.e., GaN substrate, in the shape of a bar by the cleavage, forming both the resonators end face and giving end-face coating further to these resonator end faces, this bar is chip-ized by the cleavage. GaN system semiconductor laser of SCH structure made into the purpose is manufactured by the above.

[0033] As mentioned above, according to this 1st operation gestalt, when opening 4a of an equilateral-triangle pattern which has symmetric property symmetrical with 3 times carries out the selective growth of the GaN layer 5 using the growth mask 4 which has the mask pattern arranged through mask section 4b, the stress by the coefficient-of-thermal-expansion difference with Cth page silicon on sapphire 1 is eased, and this GaN layer 5 can stop curvature and crack initiation. For this reason, even if it grows up the GaN layer 5 of a thick film, occurrence of the crack or curvature can be prevented effectively and the GaN layer 5 of a quality single crystal can be obtained. Thus, by the ability preventing the crack of the GaN layer 5, and occurrence of curvature, in order to take only the GaN layer

5, to come out and to carry out, in case a wrapping removes Cth page silicon on sapphire 1, there is no problem on which a chip and a crack increase, and GaN substrate can be manufactured by the high yield. And by growing up GaN system semiconductor layer which forms laser structure, forming the ridge section further, and forming the p lateral electrode 13 and the p lateral electrode 14 on GaN substrate which does in this way and is obtained GaN system semiconductor laser which has the structure where p lateral electrode was formed in the element front face, and n lateral electrode was formed in the substrate rear face like GaAs system semiconductor laser can be efficiently manufactured by the high yield by resonator end-face formation by the usual cleavage. Moreover, since GaN substrate is flat, the problem that it cannot correspond to curvature does not have the depth of focus of an aligner at the time of the exposure in the photo-lithography process performed after a crystal growth, either. Furthermore, degree of freedom in the manufacturing process of GaN system semiconductor laser can be made high by using GaN substrate.
[0034] Next, the manufacture technique of GaN system semiconductor laser by the 2nd operation gestalt of this invention is explained.
[0035] In this 2nd operation gestalt, the thing of a pattern configuration which is shown in drawing 9 is used as a growth mask 4 formed on the substratum GaN layer 3. As shown in drawing 9 , this growth mask 4 has the mask pattern by which opening 4a of a right hexagonal-method pattern which has symmetric property symmetrical with 6 times was arranged through mask section 4b of predetermined width of face. The side of opening 4a of the right hexagonal method of this growth mask 4 is made to become parallel to the <11-20> orientation of Cth page silicon on sapphire 1, or the <1-100> orientation here. Moreover, the length of the side of opening 4a of the right hexagonal method of this growth mask 4 is set to 7 micrometers, and width of face of mask section 4b between them is set to 3 micrometers. Since other things are the same as that of the 1st operation gestalt, they omit an explanation.
[0036] Also according to this 2nd operation gestalt, the same advantage as the 1st operation gestalt can be acquired.
[0037] Next, the manufacture technique of GaN system semiconductor laser by the 3rd operation gestalt of this invention is explained.
[0038] In this 3rd operation gestalt, as shown in drawing 10 , the growth mask 4 is directly formed on Cth page silicon on sapphire 1. As this growth mask 4, the thing of a mask pattern which is shown in the drawing 3 or the drawing 9 is used. And the selective growth of the GaN layer 5 is carried out on Cth page silicon on sapphire 1 using this growth mask 4. Since other things are the same as that of the 1st operation gestalt, they omit an explanation.
[0039] Also according to this 3rd operation gestalt, the same advantage as the 1st operation gestalt can be acquired, and also by carrying out the selective growth of the GaN layer 5 directly on the Cth page silicon on sapphire 1 in which the growth mask 4 was formed, growth required for a manufacture of GaN substrate can be managed at once, therefore can acquire the advantage that a reduction of the manufacturing cost of GaN system semiconductor laser can be aimed at.
[0040] As mentioned above, although the operation gestalt of this invention was explained concretely, this invention is not limited to the above-mentioned operation gestalt, and various kinds of deformation based on the technical thought of this invention is possible for it.
[0041] for example, the 1- it may not pass over the numeric value mentioned in the 3rd operation gestalt, structure, a substrate, a raw material, a process, etc. for an example to the last, but the numeric value different from these, structure, a substrate, a raw material, a process, etc. may be used if needed
[0042] concrete -- the 1- in the 3rd operation gestalt, although the HVPE method is used for the selective growth of the GaN layer 5, you may use the MOCVD method and the MBE method instead of the HVPE method if needed Moreover, you may use the MBE method and the HVPE method for growth of GaN system semiconductor layer which forms GaN buffer layer 2, the substratum GaN layer 3, and laser structure instead of the MOCVD method.
[0043] furthermore, the 1- in the 3rd operation gestalt, although the case where this invention was applied to a manufacture of GaN system semiconductor laser was explained, this invention may be applied to a manufacture of GaN system light emitting diode, and may be further applied to a manufacture of GaN system electronic run elements, such as GaN system FET
[0044]
[Effect of the Invention] As explained above, even if it grows up the thick film of semiconductors, such as a nitride system III-V group compound semiconductor, on the substrate from which a lattice constant and a coefficient of thermal expansion are different by using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part according to this invention, it can prevent that curvature and a crack occur. And a semiconductor substrate can be manufactured using the semiconductor layer of the thick film by which a selective growth is carried out by doing in this way, and various kinds of semiconductor devices can be further manufactured using this semiconductor substrate.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] Especially this invention is applied to a manufacture of the semiconductor laser, the light emitting diode, or the electronic run element using the nitride system III-V group compound semiconductor about the growth technique of a semiconductor, the manufacture technique of a semiconductor substrate, and the manufacture technique of a semiconductor device, and is suitable.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] In recent years, the development of semiconductor light emitting devices, such as semiconductor laser which can obtain the photogenesis to an ultraviolet region from a visible region, and light emitting diode, is actively performed using nitride system III-V group compound semiconductors, such as AlGaInN. It is asked for utilization of the semiconductor laser from which photogenesis of a short wavelength region is obtained in order to raise recording density, such as an optical disk, in the field of optical recording also especially in it.
[0003] Recently, in AlGaInN system semiconductor laser, the continuous oscillation of 300 hours in a room temperature is attained by growing up a nitride system III-V group compound semiconductor layer by the organic metalization study vapor-growth (MOCVD) method through the buffer layer which consists of a gallium nitride (GaN) on silicon on sapphire (Jpn.J.Appl.Phys.35, L74 (1996), Jpn.J.Appl.Phys.36, L1059 (1997)). However, the nitride system III-V group compound semiconductor layer grown up on silicon on sapphire since silicon on sapphire differed also in a lattice constant and a coefficient of thermal expansion greatly from GaN is 1x108 to 1x109. An individual / cm2 It has the penetration trusion (trusion which the trusion defect spread and ran through under the crystal) of a grade, and when this produces a light emitting device, it is the factor which determines the life. Therefore, in order to realize the practical life of 10,000 hours or more, it is required to reduce the density of this penetration trusion, and various studies are made until now.
[0004] For example, although one of them has use of GaN substrate The technique of the present leading ** being carried out as the manufacture technique of GaN substrate Grow up GaN layer through a buffer layer on silicon on sapphire, and the growth mask which formed the silicon-dioxide (SiO2) layer of the shape of a stripe of 1-4 micrometer width of face in the 7-micrometer pitch is formed on it. After making longitudinal direction carry out the selective growth of the GaN layer by the chloride vapor-phase-epitaxial-growth method on silicon on sapphire using this growth mask, GaN substrate is manufactured by removing silicon on sapphire (Jpn.J.Appl.Phys.36 and L899 (1997)). It is the density of the penetration trusion of GaN layer which grew on the growth mask according to this technique, i.e., GaN substrate, 1x107 An individual / cm2 It can decrease even to a grade.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, even if it grows up the thick film of semiconductors, such as a nitride system III-V group compound semiconductor, on the substrate from which a lattice constant and a coefficient of thermal expansion are different by using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part according to this invention, it can prevent that curvature and a crack occur. And a semiconductor substrate can be manufactured using the semiconductor layer of the thick film by which a selective growth is carried out by doing in this way, and various kinds of semiconductor devices can be further manufactured using this semiconductor substrate.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the manufacture technique of the above-mentioned conventional GaN substrate, asymmetry by the coefficient-of-thermal-expansion difference with silicon on sapphire becomes large as a growth thickness increases, although it decreases, and curvature and a crack produce the density of the penetration trusion of a growth phase at the time of the temperature fall after a crystal growth. For this reason, a chip and a crack will increase at the time of a wrapping at the elimination process of silicon on sapphire, and the manufacture yield of a substrate will become very low. Moreover, when a light emitting device was produced on this GaN substrate that curved, there were various problems -- the depth of focus of an aligner cannot correspond to curvature -- at the time of the exposure in the photo-lithography process performed after a crystal growth.
[0006] Therefore, even if the purpose of this invention grows up the thick film of semiconductors, such as a nitride system III-V group compound semiconductor, on the substrate from which a lattice constant and a coefficient of thermal expansion are different, it is to offer the growth technique of the semiconductor which neither curvature nor a crack generates, the manufacture technique of the semiconductor substrate using this growth technique, and the manufacture technique of a semiconductor device.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] If according to the study of this invention person the crack and curvature of the growth phase which is the trouble of the above-mentioned conventional technique have the critical point in the stress generated in the growth phase according to the coefficient-of-thermal-expansion difference with a substrate and stress exceeds it, a crack will arise in a growth phase, and when stress is less than [it], it is discovered as curvature. And as a result of inquiring zealously, it found out that it was regular in the orientation which this crack produces. Specifically by the growth phase which consists of nitride system III-V group compound semiconductors, such as GaN, it found out generating a crack in parallel with the {11-20} **** or {1-100} ****. Moreover, when this invention person grew up the semiconductor alternatively through the growth mask which has a stripe-like pattern, he found out that the crack of the orientation in alignment with the stripe decreased.

[0008] The crack and curvature of a growth phase decrease sharply by forming a growth mask so that the plane of composition of the nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side from these things. What specifically consists of a pattern which has the symmetry or symmetric property symmetrical with 6 times 3 times as such a growth mask is effective.

[0009] Furthermore, the above thing may be similarly materialized, when growing up semiconductors other than a nitride system III-V group compound semiconductor, as long as the same property is shown.

[0010] This invention is thought out based on the above studies by this invention person.

[0011] That is, in order to attain the above-mentioned purpose, it is characterized by for invention of the 1st of this invention using a growth mask, and using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part in the growth technique of a semiconductor of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor.

[0012] It is characterized by invention of the 2nd of this invention using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part in the manufacture technique of a semiconductor substrate of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.

[0013] It is characterized by invention of the 3rd of this invention using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part in the manufacture technique of a semiconductor device of having been made to carry out the selective growth of the semiconductor on the substrate which consists of a material different from this semiconductor using a growth mask.

[0014] In this invention, what consists of a repeat pattern of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask typically is used. Although this growth mask consists only of what consists only of a pattern which has symmetric property symmetrical with 3 times, and a pattern which has symmetric property symmetrical with 6 times, the pattern which has symmetric property symmetrical with others and 3 times, and the pattern which has symmetric property symmetrical with 6 times may be intermingled.

[0015] Typically in this invention, the semiconductor which should carry out a selective growth is a nitride system III-V group compound semiconductor. Specifically, this nitride system III-V group compound semiconductor consists of at least one kind of III group element chosen out of the group which consists of a gallium (Ga), aluminum (aluminum), an indium (In), boron (B), and a thallium (Tl), and a V group element which contains an arsenic (As) or Lynn (P) further by the case, including nitrogen (N) at least. When the example of this nitride system III-V group compound semiconductor is given, they are GaN, AlGaN, AlN, GaInN, AlGaInN, InN, etc.

[0016] In this invention, the halide vapor-phase-epitaxial-growth method (a chloride vapor-phase-epitaxial-growth method is the kind) a growth rate is quick, or a hydride vapor-phase-epitaxial-growth method (all are called "HVPE method".) is suitably used for the selective growth of a nitride system III-V group compound semiconductor. Here, a halide vapor-phase-epitaxial-growth method means the vapor growth which a halogen contributes to transportation or a reaction. You may use an organic metalization study vapor-growth (MOCVD) method, a molecular-beam-epitaxy (MBE) method, etc. for the selective growth of a nitride system III-V group compound semiconductor.

[0017] In this invention, although what was chosen as a substrate according to the semiconductor which should carry out a selective growth is used, when carrying out the selective growth of the nitride system III-V group compound semiconductor especially, what consists of sapphire, silicon carbide (SiC), a zinc oxide (ZnO), a spinel, silicon (Si), a **-ized gallium (GaAs), etc. is used suitably. As a growth mask, specifically Moreover, a dielectric (SiO2), for example, a silicon dioxide, What consists of silicon nitride (SiN), an aluminum oxide (aluminum2 O3), etc., The cascade screen of at least two layers chosen out of the group which consists of a layer of these dielectrics, IVa group's metals (Ti, Zr, Hf, etc.), and Va group's metal (it Nbs V --) What [consists of the metal membrane or alloy layer which consists of at least one kind of metals chosen out of the group which consists of VIa group's metals (Cr, Mo, W, etc.) and nickel, such as Ta,] What consists of a cascade screen of the metal membrane or alloy layer which consists of at least one kind of metal

chosen out of the group which consists of IVa group's metal, Va group's metal, VIa group's metal, and nickel, and a dielectric film is used.

[0018] In this invention, when the semiconductor which should carry out a selective growth is a nitride system III-V group compound semiconductor, a growth mask is formed so that the plane of composition of the nitride system III-V group compound semiconductor which carries out a selective growth may turn into {11-20} side or {1-100} side.

[0019] In the 2nd of this invention, and the 3rd invention, typically, after carrying out the selective growth of the semiconductor, a wrapping, etching, etc. remove a substrate.

[0020] In this invention constituted as mentioned above By using the growth mask which contains at least the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times as a growth mask in part When the selective growth of the nitride system III-V group compound semiconductor is carried out on a substrate using this growth mask, In the fraction of the pattern which has the symmetry or symmetric property symmetrical with 6 times about 3 times among growth masks at least Since the plane of composition of the nitride system III-V group compound semiconductor which carries out a selective growth turns into {11-20} side or {1-100} side from each opening of a growth mask, the stress by the coefficient-of-thermal-expansion difference with a substrate is eased, and a growth phase can reduce curvature and crack initiation. For this reason, even if it grows up a thick film, occurrence of the crack or curvature can be prevented.

[0021]

[Embodiments of the Invention] Hereafter, it explains, referring to a drawing about the operation gestalt of this invention. In addition, in the complete diagram of the operation gestalt, the same sign is given to an identity or a corresponding fraction.

[0022] First, the manufacture technique of GaN system semiconductor laser by the 1st operation gestalt of this invention is explained. This manufacture technique is shown in drawing 1 - view 8 . This GaN system semiconductor laser has SCH (Separate Confinement Heterostructure) structure.

[0023] In this 1st operation gestalt, first, as shown in drawing 1 , Cth page silicon on sapphire 1 is prepared, and thickness grows up GaN buffer layer 2 which is 30nm at the temperature of 520 degrees C for example, by the MOCVD method on it. This GaN buffer layer 2 consists of a near crystal layer amorphously, and serves as the nucleus at the time of growing up a substratum layer on it. In growth of this GaN buffer layer 2, trimethylgallium (CH_3) (3 Ga) gas and ammonia (NH_3) gas are used as material gas, for example. Next, thickness grows up the substratum GaN layer 3 which is 2 micrometers at the temperature of 1020 degrees C for example, by the MOCVD method on this GaN buffer layer 2.

[0024] Next, SiO_2 whose thickness is 0.1 micrometers at the temperature of 450 degrees C by CVD on the substratum GaN layer 3 as shown in drawing 2 This SiO_2 after forming a layer Patterning of the layer is carried out by the photo-lithography method and the etching method, and the growth mask 4 of a pattern configuration which is shown in drawing 3 is formed. As shown in drawing 3 , this growth mask 4 has the mask pattern by which opening 4a of an equilateral-triangle pattern which has symmetric property symmetrical with 3 times was arranged through mask section 4b of predetermined width of face. The side of the pattern of the equilateral triangle which constitutes this growth mask 4 is made to become parallel to the <11-20> orientation of Cth page silicon on sapphire 1, or the <1-100> orientation here. Moreover, the length of the side of opening 4a of the equilateral triangle of this growth mask 4 is set to 7 micrometers, and width of face of mask section 4b between them is set to 3 micrometers.

[0025] Next, an acetone (CH_3COCH_3) and a methanol (CH_3OH) wash the Cth page silicon on sapphire 1 in which the growth mask 4 was formed, and further, after dipping in the diluted hydrochloric acid (HCl) or the diluted fluoric acid (HF) about 10 seconds, a pure water washes, for example.

[0026] Next, as shown in drawing 4 , the selective growth of the GaN layer 5 is carried out to longitudinal direction at the temperature of 1000 degrees C by the chloride vapor-phase-epitaxial-growth method, using the growth mask 4. In the selective growth of this GaN layer 5, after, heating Cth page silicon on sapphire 1 to 1000 degrees C for example, passing ammonia (NH_3) gas by 1l. the flow rate for /, on a metal Ga, hydrogen chloride (HCl) gas is passed and gallium-chloride (GaCl) gas is supplied. As for the conditions of supply of GaCl gas, a growth rate is made to become o'clock in about 40micrometers /. In the case of this selective growth, the plane of composition of GaN layer which carries out a selective growth to longitudinal direction on mask section 4b from on the substratum GaN layer 3 of each opening 4a of the growth mask 4 When the side of opening 4a of the equilateral triangle of the growth mask 4 is parallel to the <11-20> orientation of Cth page silicon on sapphire 1, it becomes {11-20} side of GaN. When the side of opening 4a of the equilateral triangle of the growth mask 4 is parallel to the <1-100> orientation of Cth page silicon on sapphire 1, it becomes {1-100} side of GaN. If the selective growth of the 1 hour GaN is carried out on these conditions, the GaN layer 5 of the thick film of the single crystal with thickness quality [the low crystal-defect density with a flat front face] at about 40 micrometers will be obtained. The orientation relationship of Cth page silicon on sapphire 1 and the GaN layer 5 is shown in drawing 5 .

[0027] Thus, the place, the curvature, or crack initiation which observed the GaN layer 5 by which the selective growth was carried out with the light microscope were not seen.

[0028] Next, as shown in drawing 6 , by wrapping mechanically, it removes and only the GaN layer 5 by which the selective growth was carried out is taken out for Cth page silicon on sapphire 1 etc. from the rear-face side.

[0029] Next, as shown in drawing 7 , the GaN layer 5 of the thick film which does in this way and was obtained is used as a GaN substrate. On it by for example, the MOCVD method The n type AlGaN clad layer 6, the n type GaN lightguide 7 8, for example, the barrier layer of $Ga_{1-x}In_xN/Ga_{1-y}In_yN$ multiplex quantum well structure, the p type AlGaN cap layer 9, the p type GaN lightguide 10, the p type AlGaN clad layer 11 And the p type GaN contact layer 12 is grown up one by one. Here, since the GaN layer 5 used as the substratum of these layers is a single crystal with a quality low crystal-defect density, these layers also serve as the single crystal with a quality low crystal-defect density. Growth temperature of the n type AlGaN clad layer 6 which is a layer which does not contain In here, the n type GaN lightguide 7, the p type AlGaN cap layer 9, the p type GaN lightguide 10, the p type AlGaN clad layer 11, and the p type GaN contact layer 12 is made into about 1000 degrees C. Growth temperature of the barrier layer 8 of the $Ga_{1-x}In_xN/Ga_{1-y}In_yN$ multiplex quantum well structure which is a layer containing In is made into 700-800 degrees C. Moreover, as for example, a Ga raw material, ammonia (NH_3) is used for the growth raw material of these GaN system semiconductor layers as trimethylindium (CH_3) (3In)

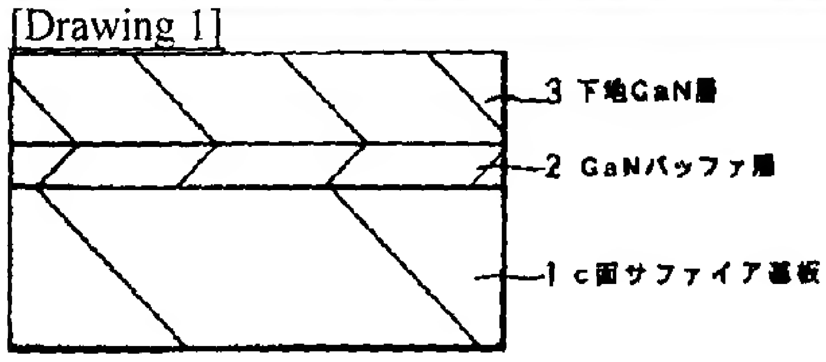
* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

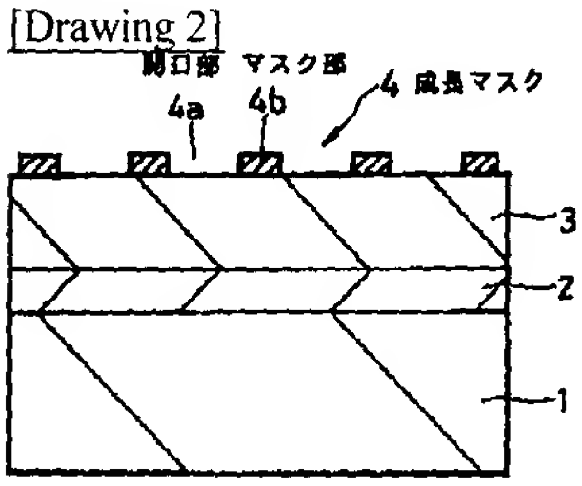
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

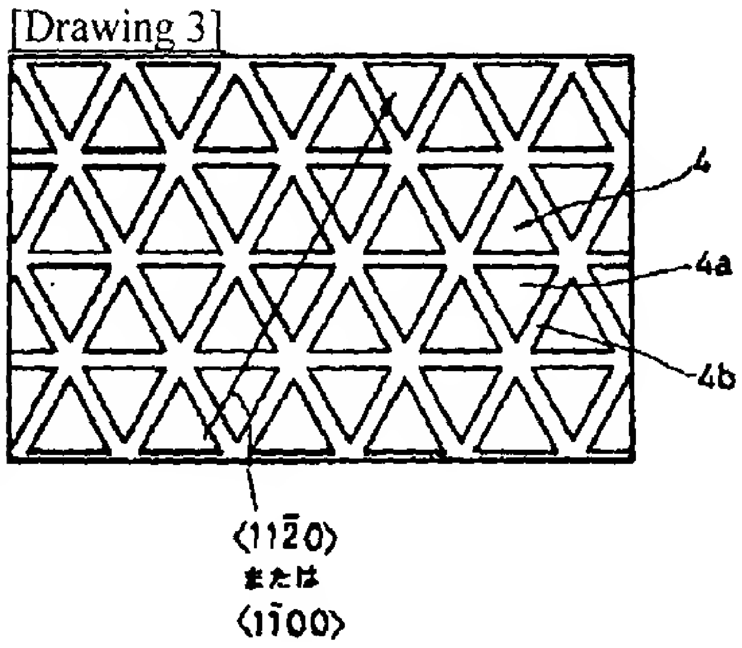
[Drawing 1]



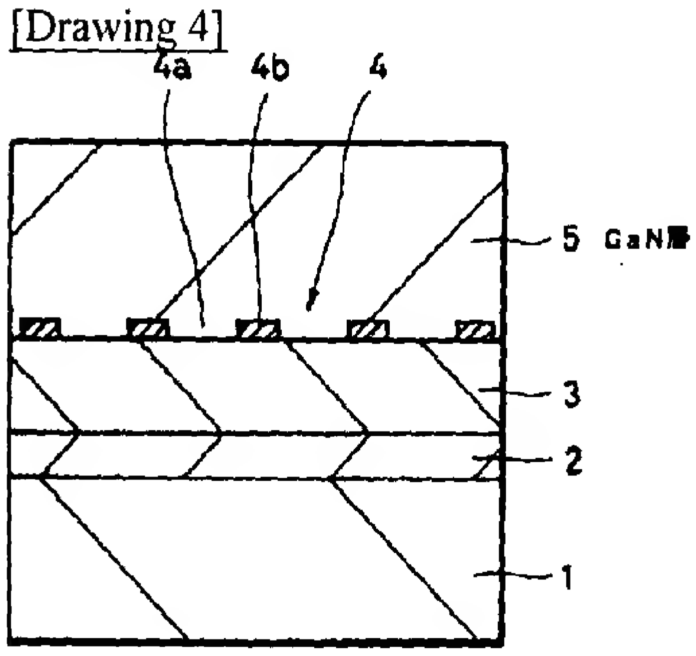
[Drawing 2]



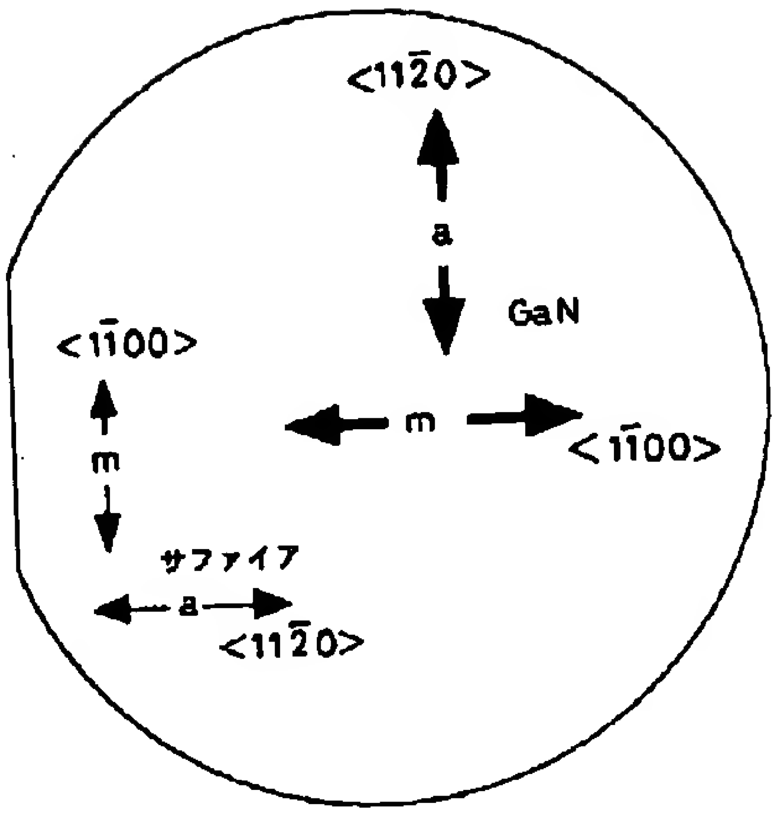
[Drawing 3]



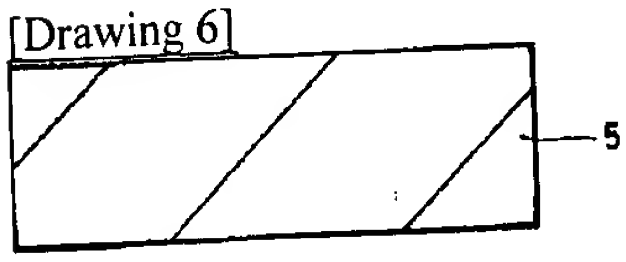
[Drawing 4]



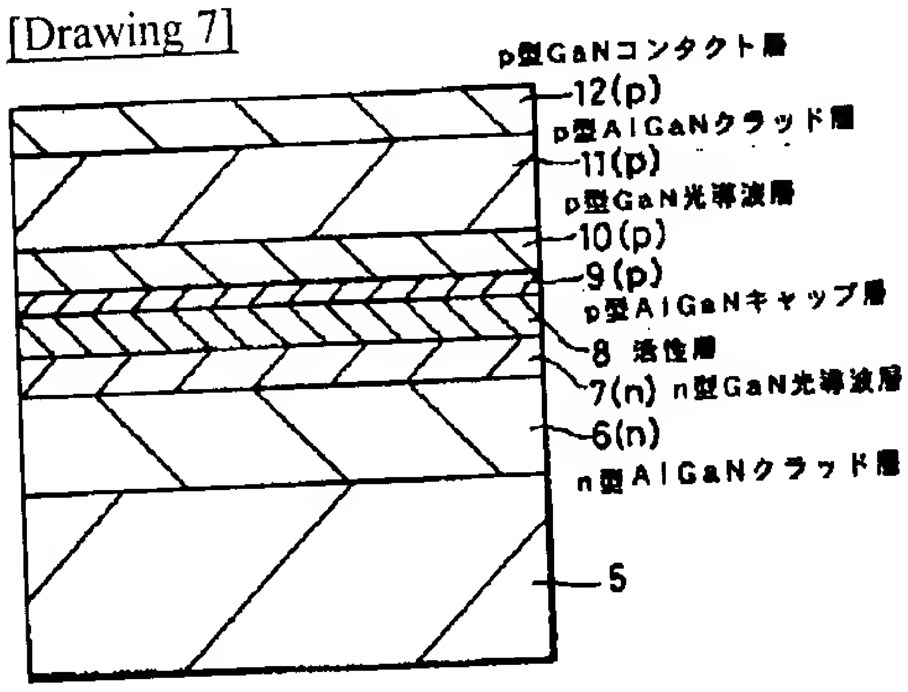
[Drawing 5]



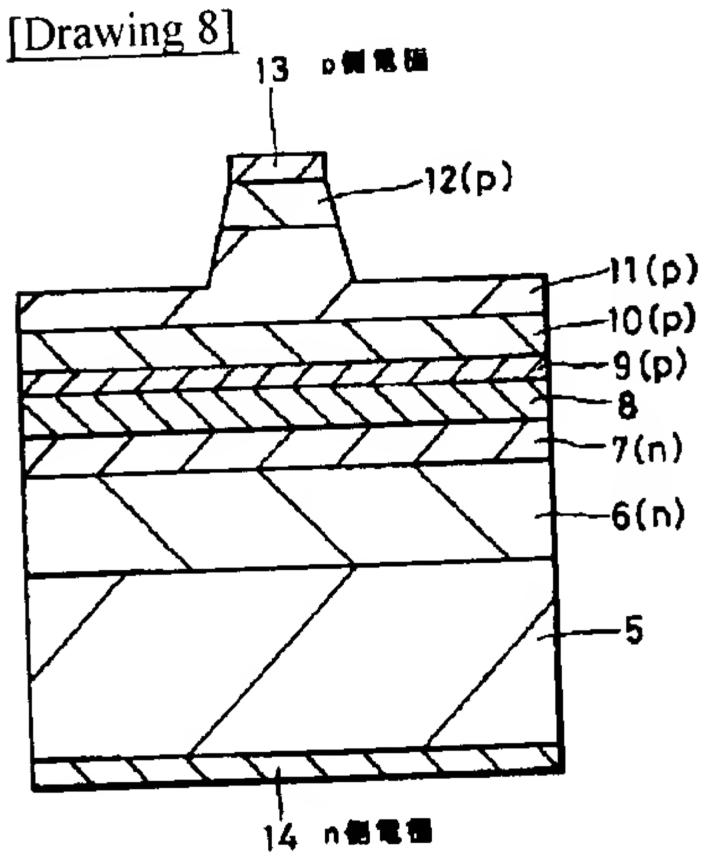
[Drawing 6]



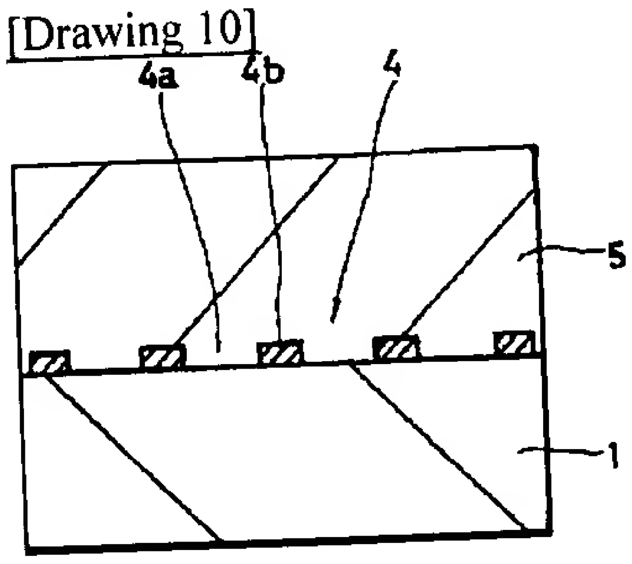
[Drawing 7]



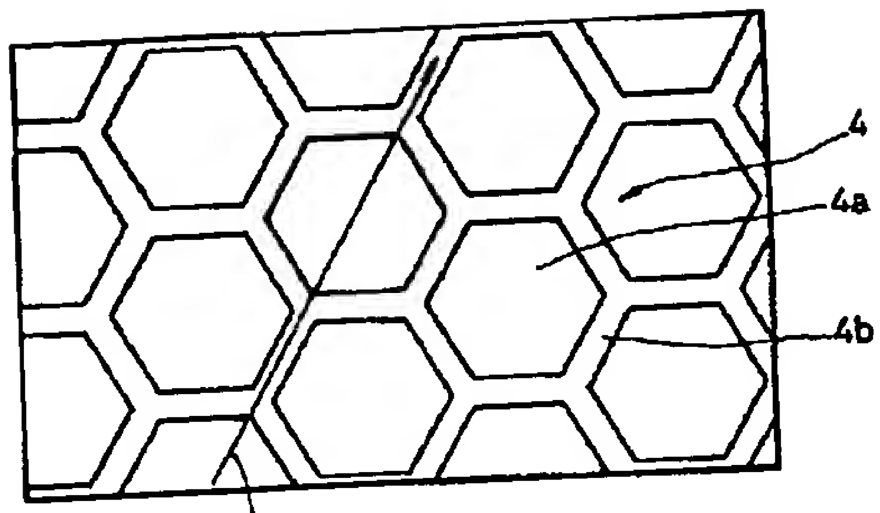
[Drawing 8]



[Drawing 10]



[Drawing 9]



[Translation done.]

US 096800540AP1

Creation date: 09-11-2003
Indexing Officer: HNGUYEN13 - HIEU NGUYEN
Team: OIPEBackFileIndexing
Dossier: 09680054

Legal Date: 09-09-2002

No.	Doccode	Number of pages
1	A...	1
2	CLM	4
3	REM	9
4	LET.	3

Total number of pages: 17

Remarks:

Order of re-scan issued on ....